

1 CLAIMS

2 We Claim:

3

4 1. An input/output circuit for an integrated circuit
5 comprising:

6 an input pad;

7 a follower circuit coupled to the input pad;

8 a pull-up circuit coupled to the input pad; and

9 a pull-down circuit coupled to the input pad.

10

11 2. A method for an input/output circuit for an
12 integrated circuit comprising:

13 tri-stating an output buffer; and

14 providing one of a weak pull-up, a weak pull-
15 down, and a pad signal follower on an input pad.

16

17 3. An input/output circuit for an integrated circuit
18 comprising:

19 an input pad;

20 a pull-up circuit coupled to the input pad;

21 a first multiplexer having a control terminal
22 receiving values from a first plurality of memory
23 cells, the first multiplexer having a first output
24 signal coupled to a control terminal of the pull-up
25 circuit;

26 a pull-down circuit coupled to the input pad;

27 a second multiplexer having a control terminal
28 receiving values from a second plurality of memory
29 cells, the second multiplexer having a second output
30 signal coupled to a control terminal of the pull-down
31 circuit;

32 a tri-state buffer coupled to the input pad;

1 a third multiplexer having a control terminal
2 receiving a value from a first memory cell at a first
3 input terminal and receiving a first user-defined
4 value at a second input terminal, the third
5 multiplexer having a third output signal coupled to an
6 enable terminal of the tri-state buffer; and
7 a fourth multiplexer having a control terminal
8 receiving a value from a second memory cell at a first
9 input terminal and receiving a second user-defined
10 value at a second input terminal, the fourth
11 multiplexer having a fourth output signal coupled to a
12 data output terminal of the tri-state buffer;
13 wherein a configuration signal from a user-defined
14 logic circuit is provided to the control terminals of the
15 first, second, third, and fourth multiplexers.

16

17 4. A method for an input/output circuit for an
18 integrated circuit comprising:
19 providing a pull-up circuit to an input pad of the
20 input/output circuit;
21 using a configuration signal to select between a first
22 plurality of memory cells, thereby controlling the pull-up
23 circuit;
24 providing a pull-down circuit to an input pad of the
25 input/output circuit;
26 using the configuration signal to select between a
27 second plurality of memory cells, thereby controlling the
28 pull-down circuit;
29 providing control signals to a tri-state buffer
30 coupled to the input pad; and

1 using the configuration signal to select between a
2 plurality of signals used to control define the control
3 signals.

4

5 5. A method for providing a minimal hold time
6 relative to a fixed global clock for the data provided to
7 an input/output circuit of a programmable integrated
8 circuit, the method comprising:

9 providing a fixed clock signal to the
10 input/output circuit;

11 providing a data signal to the input/output
12 circuit;

13 receiving the data signal with a programmable
14 delay circuit; and

15 providing the delayed data signal to an input
16 register.

17

18 6. The method of Claim 5 further including the step
19 of controlling the amount of delay in the programmable
20 delay circuit with values stored in memory cells.

21

22 7. A circuit for delaying a data input signal to an
23 input/output circuit of an integrated circuit comprising:

24 a plurality of memory cells;

25 a delay structure having control inputs coupled
26 to the plurality of memory cells;

27 a data input pad for receiving a data input
28 signal coupled to a data input terminal of the delay
29 structure;

30 a clock distribution system having a fixed delay;

1 a clock input pad for receiving a clock input
2 signal coupled to an input terminal of the clock
3 distribution system;

4 a multiplexer having a first input terminal
5 coupled to an output terminal of the input delay
6 system and having a second input terminal coupled to
7 the data input pad;

8 a first memory cell coupled to a control terminal
9 of the multiplexer; and

10 an input register having a data input terminal
11 coupled to an output terminal of the multiplexer and
12 having a clock input terminal coupled to an output
13 terminal of the clock distribution system.

14
15 8. A circuit for delaying a data signal comprising:

16 a first inverter;

17 a second inverter coupled to an output terminal
18 of the first inverter;

19 a first plurality of p-channel transistor pairs
20 coupled between a first supply voltage and a first
21 supply rail of the first inverter, one of each
22 transistor pair having a gate coupled to a second
23 supply voltage;

24 a first plurality of n-channel transistor pairs
25 coupled between a third supply voltage and a second
26 supply rail of the first inverter, one of each
27 transistor pair having a gate coupled to a fourth
28 supply voltage;

29 a first capacitor pair having a control terminal
30 coupled to an output terminal of the second inverter;

31 a third inverter coupled to the control terminal
32 of the first capacitor pair;

1 a second plurality of p-channel transistor pairs
2 coupled between a fifth supply voltage and a first
3 supply rail of the third inverter, one of each
4 transistor pair having a gate coupled to a sixth
5 supply voltage;

6 a first plurality of n-channel transistor pairs
7 coupled between a seventh supply voltage and a second
8 supply rail of the third inverter, one of each
9 transistor pair having a gate coupled to a eighth
10 supply voltage;

11 a second capacitor pair having a control terminal
12 coupled to an output terminal of the third inverter;
13 and

14 a fourth inverter coupled to an output terminal
15 of the third inverter.

16
17 9. A method for delaying a data signal comprising:
18 providing a data signal to a delay circuit;
19 buffering the data signal;
20 inverting the data signal with an inverter having
21 supply rails supplied by series resistor circuits;
22 passing the data signal through a capacitor pair;
23 inverting the data signal with an inverter having
24 supply rails supplied by series resistor circuits;
25 passing the data signal through a capacitor pair;
26 and
27 buffering the data signal.

28
29 10. A circuit for testing an input/output circuit
30 comprising:

31 a multiplexer coupled to a horizontal bus;
32 a multiplexer coupled to a vertical bus;

1 an OR gate having a first input terminal coupled
2 to the first multiplexer and a second input terminal
3 coupled to the second multiplexer;
4 wherein the output terminal of the OR gate is coupled
5 to an input of the input/output circuit.

6

7 11. A method of testing an input/output circuit, the
8 method comprising:

9 providing a first signal from a horizontal bus;
10 providing a second signal from a vertical bus;
11 coupling the first and second signals into a
12 third signal; and
13 providing the third signal to an input of the
14 input/output circuit.

15

16 12. A circuit for transferring data from a first data
17 input pad to a second data input pad comprising:

18 a transistor; and

19 a buffer having an output terminal coupled to the
20 transistor, having a first source/drain region coupled
21 to the first data input pad, and having a second
22 source/drain region coupled to the second data input
23 pad;

24 wherein a control signal provided from the buffer to
25 the transistor either couples or de-couples the first and
26 second input pads.

27

28 13. A method for transferring data from a first data
29 input pad to a second data input pad, the method comprising
30 providing a control signal to a first transistor switch,
31 thereby coupling or de-coupling the first and second input
32 pads.

1

2 14. A method of increasing the number of channels
3 available for a direct input/output connection to an
4 input/output circuit for an integrated circuit comprising:

5 providing a bypass signal to a first input
6 terminal of an OR gate;

7 providing an output enable signal to a second
8 input terminal of the OR gate;

9 providing an output signal of the OR gate to a
10 gate of a transistor;

11 providing an input data signal to a source of the
12 transistor;

13 providing the signal at a drain of the transistor
14 to a storage latch;

15 providing an output signal of the storage latch
16 to a first route of a routing structure; and

17 providing the input data signal to a second route
18 of the routing structure.

19

20 15. An edge-placed I/O tile structure comprising:

21 an OR gate;

22 a horizontal channel multiplexer coupled to a
23 first input terminal of the OR gate;

24 a vertical channel multiplexer coupled to a
25 second input terminal of the OR gate; and

26 an I/O circuit coupled to an output terminal of
27 the OR gate.

28

29 16. The edge-placed tile structure of Claim 14
30 further comprising a second identical edge-placed tile
31 structure.